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High-speed electronics for silicon photonics transceivers

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ABSTRACT

High-speed electronic integrated circuits are essential to the development of new fiber-optic communication systems. As a consequence of the increasing speeds and multi-channel operation, close integration and co-design of photonic and electronic devices have become a necessity to realize high-performance sub-systems. Such co-design on the other hand also enables the design of new electro-optic architectures to create and process multi-level optical signals. This presentation will illustrate a number of recent and ongoing developments in IDLab, an imec research group, from various H2020 projects with a focus on application-specific high-speed electronic transceiver circuits such as driver amplifiers and transimpedance amplifiers (TIAs).

Keywords: Optical transceiver, integrated circuit, high-speed electronics, modulator driver, transimpedance amplifier, silicon photonics, SiGe BiCMOS

1. INTRODUCTION

High-speed transceivers need to scale up to follow the increasing demand of data intensive applications such as cloud services, video streaming, virtual reality, high-performance computing, 5G, etc. pushing the speeds of all sorts of interconnects and interfaces. The Ethernet Alliance is for example, working on 800 Gb/s and 1.6 Tb/s standards for multi-channel datacenter optical interconnects, whereas long-reach coherent applications will be using 400 Gb/s or 800 Gb/s per optical carrier[1].

Si photonics has been widely recognized as an attractive technology for integrating optical transceivers. With this technology, compact and low-power transceivers can be implemented at low cost and at high volume, by leveraging existing CMOS fabrication infrastructure. Moreover, the capabilities and functionality of Si photonic transceivers can be extended by postprocessing through e.g. transfer printing of III-V devices on top of the silicon to integrate e.g. lasers, amplifiers or photodiodes (PDs)[2].

To realize high-performance transceivers with low-power consumption, co-design and co-integration with high-speed electronic circuits such as driver amplifiers and TIAs is crucial. One of the main considerations at high-speed is the optimization of the interface between the modulator and its driver in the transmitter, and between the PD and its TIA in the receiver. More in particular, the interfacing must also consider the appropriate biasing of the modulator and the PD. Fully differential driver and TIA chips were recently demonstrated combining the advantages of differential circuits with novel biasing schemes to make such differential operation possible, in particular for electro-absorption modulators (EAMs) and PDs. These differentials driver and TIA circuits were co-integrated with silicon photonic transmitters and receivers and demonstrated in various NRZ (up to 70 and 90Gb/s resp.) and PAM-4 links (up to 53GBaud). Section 2 presents the differential EAM driver[3], Section 3 presents a PAM-4 transmitter based on the same EAM driver[4,5], whereas Section 4 discusses a differential linear TIA suited for both NRZ and PAM-4 modulation[7,8]. For radio-over-fiber communications, a narrowband optical receiver was developed with a custom high-linearity GaAs LNA[9], discussed in Section 6.

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2. SIGE BICMOS MULTI-CHANNEL EAM DRIVER

2.1 Introduction

This section presents a 70Gb/s capable optical transmitter consisting of a 50 μm long GeSi EAM and a fully differential driver in a 55 nm SiGe BiCMOS technology[3]. The driver is capable of delivering 2 Vpp, resulting in a 4 dB optical extinction ratio. At a wavelength of 1560 nm, open eye diagrams for 70 Gb/s after transmission over 2 km standard single-mode fiber were demonstrated. The total power consumption is only 61 mW, corresponding to 0.87 pJ/bit at 70 Gb/s.

2.2 Differential driver topology

The differential driver architecture is shown in Fig. 1. A modified supply network is applied in the output stage to DC-bias the modulator without an AC-coupled bias-tee. As such, the modulator is biased by the difference between the two bias voltages VBias1 and VBias2.
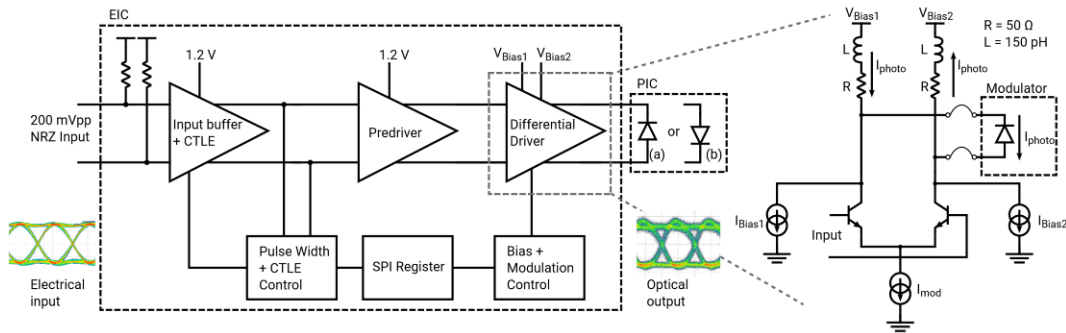

Figure 1. Left: Driver block diagram with two modulator configurations (a) and (b), Right: simplified schematic of the differential output stage with modulator biasing. For simplicity, only configuration (a) of the modulator is shown.

2.3 Realization and experimental results

The driver die micrograph and the assembly with the silicon photonic EAM are shown in Fig. 2, together with the measured optical eye diagrams up to 70 Gb/s. For these measurements, the driver output voltage was around 2 Vpp and the EAM was reverse biased around 0.9 V, created by setting VBias1 to 2 V and VBias2 to 3 V. The average EAM photocurrent sunk by the driver was around 1.5-2 mA.
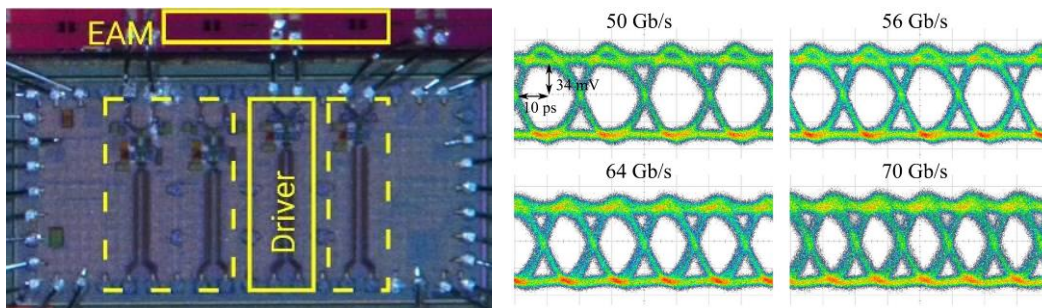

Figure 2. Left: The die micrograph and wirebonded assembly used for the electro-optical experiments. Right: measured eye diagrams up to 70 Gb/s

3. EAM-BASED OPTICAL DAC WITH CO-INTEGRATED DRIVER

3.1 Introduction

In this section, we present a 53 GBaud PAM-4 transmitter, based on two binary driven EAMs in an Mach–Zehnder interferometer configuration[4,5]. The silicon photonic PIC was co-integrated with the low-power 55nm SiGe BiCMOS

driver presented in Section 2. Two driver channels were used to drive and bias the two EAMs in the transmitter. The transmitter power consumption amounts to 160mW, or 1.5pJ/bit, comprising two driver channels and heaters on the PIC, but excluding laser.

The block diagram and operating principle are depicted in Fig. 3. The input light is split in two coherent paths, with a power ratio α:1$-\alpha$, so that the EAMs in the two arms provide different signal strengths to represent optically the least-significant bit (LSB) and the most significant bit (MSB), which after coherent recombination provide for four different power levels. The DC phase shift $\Delta\varphi$ between both arms is needed to provide an additional degree of freedom to place the PAM-4 optical power levels equidistantly.
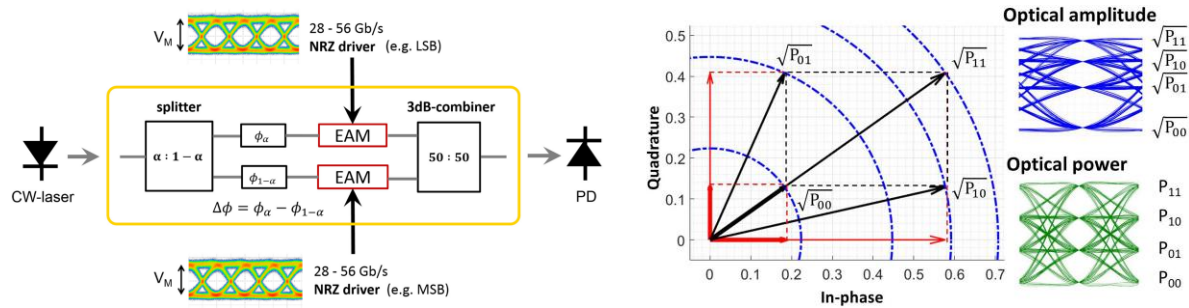

Figure 3. Left: Generalized block diagram of the PAM-4 generation topology using 2binary driven, parallel EAMs. Right: operating principle of the 2-bit optical DAC.

3.2 Realization and experimental results

The first demonstration of this concept used the architecture of Fig. 3, however, for the co-integration with the driver chip, an alternative implementation of the PIC was used by swapping the tunable splitter and 50:50 combiner, so that the input light is split equally and consequently, the EAMs produce the same average photocurrent and present the same effective average load impedance to both driver channels, preserving symmetry. The die micrographs and the wirebonded assembly are shown in Fig. 4, together with the measured optical PAM-4 eye diagram at 53 Gbaud. More results are discussed in reference[5].
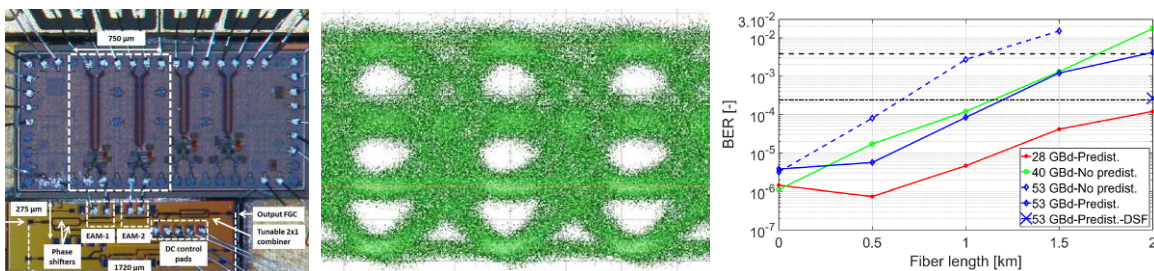

Figure 4. Left: The die micrographs and wirebonded assembly used for the electro-optical experiments. Middle: measured eye diagram at 53Gbaud PAM-4 (8 ps/div, 16 mV/div). Right: bit-error-rate, BER versus fiber length.

Another approach to apply modulators in a parallel configuration was demonstrated at 104 Gbaud PAM-4, on the same silicon photonic platform, using a pulsed laser and optical time division multiplexing[6]. The presented driver could be applied in such a scheme as well.

4. SIGE BICMOS MULTI-CHANNEL TIA

4.1 Introduction

This section presents a direct detection optical receiver that consists of a low-noise TIA, fabricated in a 55nm SiGe BiCMOS technology, and a Ge PD integrated into a silicon PIC[7,8]. Low-noise broadband operation is achieved using a fully differential TIA that provides the PD reverse bias. The circuit topology is depicted in Fig. 5. Processing the photocurrent differentially doubles the TIA gain and improves the signal-to-noise-ratio by $\sqrt{2}$. Moreover, the increased front-end gain reduces the noise contribution of the subsequent amplifying stages and also reduces their gain requirement by 6dB. This lowers the power consumption as less gain stages are required. Differential operation also improves

linearity (rejection of even harmonics), rejects common-mode noise and increases the power-supply rejection ratio (enhances stability). However, the difficulty to make a TIA differential is to provide the biasing differentially to the PD. This requires a low-noise biasing network that provides a low-impedance path for the DC photocurrent and the differential PD connection also doubles the effective PD capacitance. However, for high-speed Ge PDs this capacitance is very low anyhow.
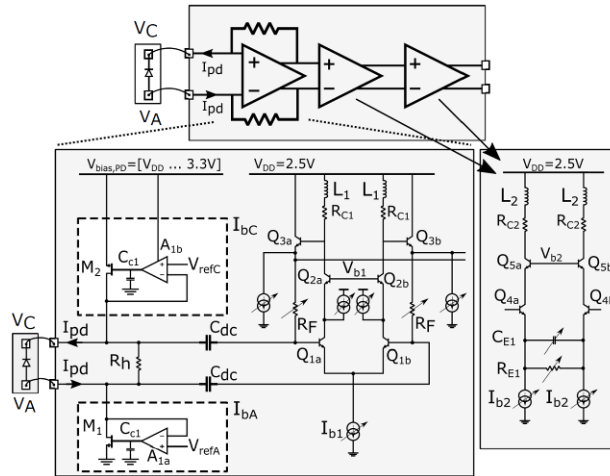

Figure 5. Block diagram of the fully differential TIA

4.2 Realization and experimental results

The TIA die micrograph and the assembly with the silicon photonic PD array are shown in Fig. 6.
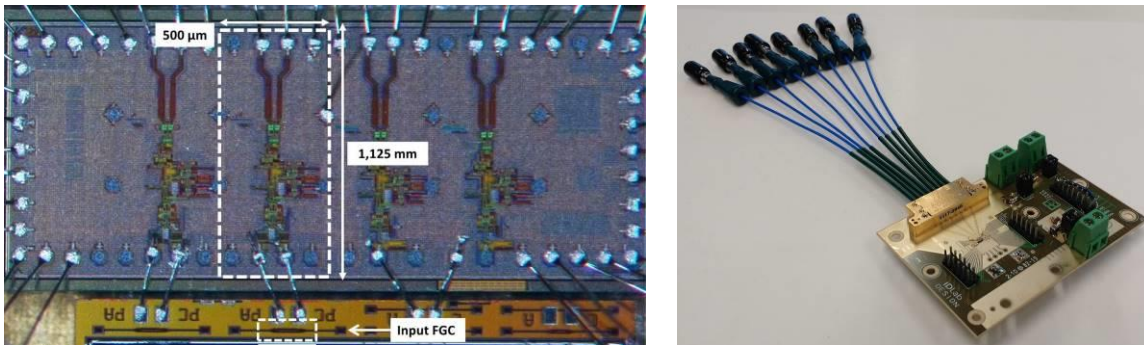

Figure 6. Left: the die micrographs and wirebonded assembly used for the electro-optical experiments. Right: high-speed connectorized test board

The BER performance was evaluated for NRZ up to 90 Gb/s, where the experiment was limited by the speed of the available transmitter, and for PAM-4 up to 53 GBaud. For NRZ, error-free operation (BER < 10^{-12}) was shown up to 80 Gb/s[7]. The TIA performance depends on the configuration settings, which allows to optimize speed or sensitivity versus power consumption. In low-power mode, the power consumption at 56 Gb/s is only 1.8 pJ/bit for -8.6dBm optical modulation amplitude (OMA) sensitivity at 10^{-12} BER. Optimizing the settings for sensitivity at 56Gb/s improves the sensitivity by 2.6 dB, at a somewhat higher power consumption of 2.5 pJ/bit. The PAM-4 eye diagrams are illustrated in Fig. 7, showing both the incoming eye from the transmitter and the eye provided by the TIA output. The BER was measured for different TIA operation modes, which allows to trade-off noise, linearity and bandwidth in order to enhance the dynamic range. At 53GBaud, a BER of 2.09x10−4 was observed at −5dBm OMA and a TIA gain of 66dBohm. BER below the forward error correction threshold of 3.8x10−3 were measured across a 7.4 dB dynamic range from −8.7dBm OMA to −1.3dBm OMA. The power consumption of the TIA in this experiment is 160mW, resulting in 1.5pJ/bit energy efficiency.

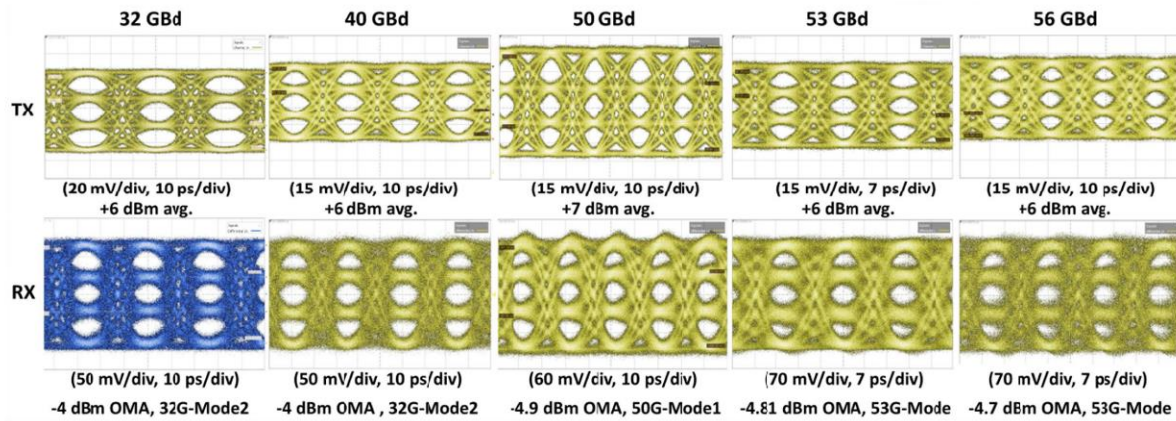|	32 GBd	40 GBd	50 GBd	53 GBd	56 GBd
TX	(20 mV/div, 10 ps/div) +6 dBm avg.	(15 mV/div, 10 ps/div) +6 dBm avg.	(15 mV/div, 10 ps/div) +7 dBm avg.	(15 mV/div, 7 ps/div) +6 dBm avg.	(15 mV/div, 10 ps/div) +6 dBm avg.
RX	(50 mV/div, 10 ps/div) -4 dBm OMA, 32G-Mode2	(50 mV/div, 10 ps/div) -4 dBm OMA , 32G-Mode2	(60 mV/div, 10 ps/div) -4.9 dBm OMA, 50G-Mode1	(70 mV/div, 7 ps/div) -4.81 dBm OMA, 53G-Mode	(70 mV/div, 7 ps/div) -4.7 dBm OMA, 53G-Mode

Figure 7. Upper row: PAM-4 eye diagrams at transmitter output. Lower row: optical receiver output eye diagrams
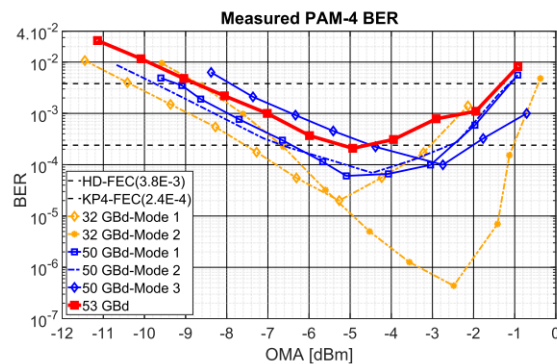

Figure 8. Measured PAM-4 BER as function of the outer OMA

5. 28GHZ RESONANT OPTICAL RECEIVER

5.1 Introduction

This section presents a photoreceiver that can be applied at the remote radio head in a 28 GHz analog RoF link[9]. The photoreceiver comprises a Ge-on-Si PD and co-designed GaAs LNA offering 24 dB gain, corresponding to 224 V/W external conversion gain, over a 3-dB bandwidth between 23.5 and 31.5 GHz. The noise figure is 2.1 dB and an output referred third order intercept point up to 26.5 dBm can be obtained with a power consumption of 303 mW.

5.2 Topology of the narrowband optical receiver

The topology of the resonant LNA is shown in Fig. 9 and consists of 3 amplification stages that can be biased independently. All three of these stages use common source amplifiers where the first two include source degeneration to bring optimal source impedances for noise and gain matching closer together. The input of the amplifier is wirebonded to a Ge-on-Si PD and is connected to V_{PD} with an internal bias tee to counter inductance variations and source DC current generated by the PD. At the output, AC coupling is present and a 50 Ω load is expected.
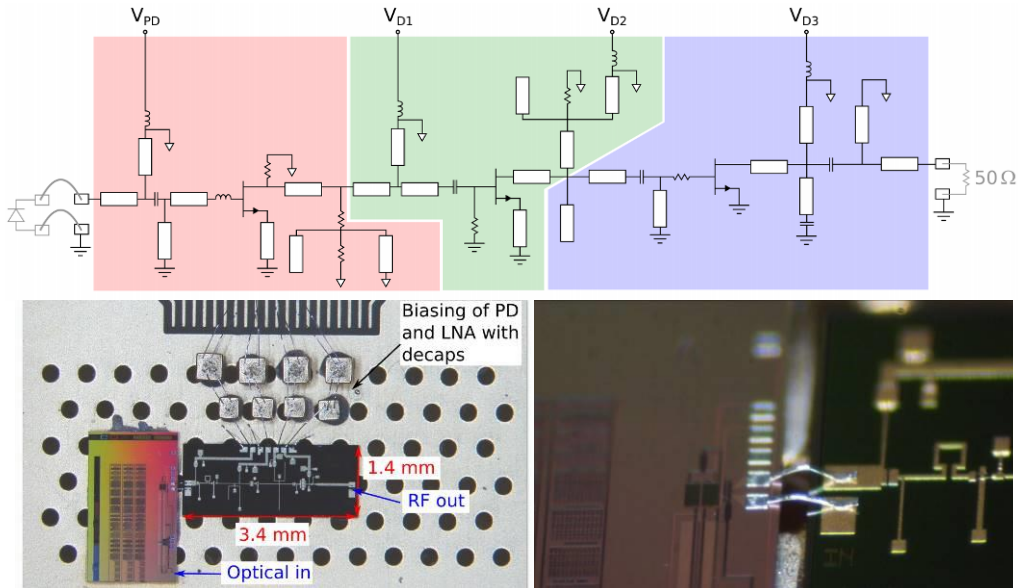
Figure 9. Top: Schematic of the narrowband mmWave photoreceiver. Bottom: Assembly

5.3 Experimental results

Two possible applications are demonstrated in reference[9]. First, the photoreceiver was tested in a 5G New Radio environment resulting in rms-EVM values below 2.46/3.47% for 100/400-MBaud 16-QAM transmission over the 24.25–29.5 GHz band, as shown in Fig. 10. Secondly, the photoreceiver was used in a high data rate link showing the potential of sending 36 Gb/s in an optical-back-to-back configuration at an rms-EVM of 5.2% (Fig. 10) and 20 Gb/s over 21 km of SSMF at an rms-EVM of 5.8%. These results showcase the capabilities of narrowband photoreceivers in extreme mobile broadband communication links for next-generation wireless communication.
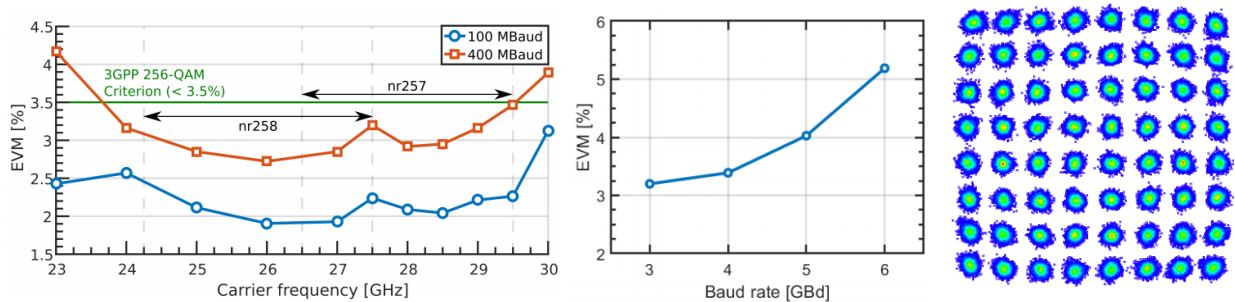

Figure 10. Photoreceiver performance (left) 5G New Radio (center) High baud rate (right) Constellation 36 Gb/s OB2B

6. CONCLUSIONS

This invited paper presented a number of state-of-the-art high-speed optical transceivers where custom developed electronic driver and TIA chips were co-integrated with co-designed silicon photonic integrated circuits. Close integration and co-design of photonic and electronic devices have become a necessity to realize high-performance sub-systems as a consequence of the increasing speeds and multi-channel operation. To further scale the capacity of optical transceivers to a next level ongoing research is exploring various ways forward for which custom high-speed electronics remains a crucial part in the development.

ACKNOWLEDGEMENTS

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